國立交通大學 106 學年度碩士班考試入學試題

科目：計算機系統(1103)　　考試日期:106年2月10日 第 3 節

系所班別：資訊聯招　　第 1 頁,共 8 頁

【不可使用計算機】＊作答前請先核對試題、答案卷(試卷)與准考證之所組別與考科是否相符！！

請用答案卡作答

一、複選題(80%)，共二十題，每題全對得 4 分。答對一個選項得 1 分(答對兩個選項得 2 分，以此類推)，答錯一個選項倒扣 2 分(答錯兩個選項倒扣 4 分，最多扣至該題 0 分為止)，整題未作答不給分。(舉例：每題有 a、b、c、d 四個選項，某題答案為 a、b，而作答時選 a、b、c，則 3 個選項正確 1 個錯誤，該題得 3-2= 1 分)。

1. Which of the following objects have identical binary representation no matter the machine is little endian or big endian.
   (a) 2's complement number -1
   (b) int i = 0xABBAABBA
   (c) A single precision number -0.0 (in IEEE754 encoding format)
   (d) A C null pointer

2. For the pipelined implementation of the MIPS processor, which statements below are NOT correct?
   (a) All pipelined registers have the same length
   (b) The pipeline clock cycle time is the average of all stage latencies.
   (c) Exceptions in a pipeline are handled like mis-predicted branches.
   (d) In the pipelined data path, separate instruction and data memories are used to reduce data hazards.

3. Assume the register numbers of $s2 and $zero are 17 and 0, respectively. Given the MIPS code sequence below, if we assume it starts at location 8000 4000h in memory, which of following statements are correct? .

```
8000 4000h
            add     $t0, $zero, $zero
loop:       beq     $s2, $zero, finish
            add     $t0, $t0, $s1
            sub     $s2, $s2, 1
            j       loop
finish:     addi    $t0, $t0, 100
            add     $v0, $t0, $zero
```

   (a) The MIPS machine codes of the ***beq*** (OP code is 4) in this code sequence is 12 20 00 03h.
   (b) The MIPS machine code of the ***j*** (OP code is 2) in this code sequence is 08 00 10 00h.
   (c) Assume both $s1 and $s2 initially contain integers 5 and 6, respectively. The value in $v0 is 30 after the execution of the whole code sequence.
   (d) With the same assumption as (c) that both $s1 and $s2 initially contain integers 5 and 6, respectively. The ***beq*** instruction will be executed 6 times for this code sequence.

4. Consider the following sequence of actual outcomes for a branch. T means the branch is taken. N means not taken. Assume both predictors are initialized to predict **taken**. Which of following statements are true?

   Branch: **T-N-T-N-N-T-N**

   (a) If 1-bit predictor is used, the predictions for this branch will be T-T-N-T-N-N-T.
   (b) If 2-bit predictor is used, the predictions for this branch will be T-T-T-T-T-N-N.
   (c) If the same pattern (i.e., T-N-T-N-N-T-N) are repeated thousands of times, the prediction accuracy rate of 1-bit predictor is about 2/7.
   (d) If the same pattern are repeated thousands of times, the prediction accuracy rate of 2-bit predictor is about 4/7.

5. Given the operation times for the major functional units are: 200ps for memory access, 100ps for ALU operation; and 50ps for register file read or write. Assuming that all the other delays (like control unit, multiplexer, pipeline overheads, etc) are negligible. Assume only R-type, lw, sw are supported. Which of

following statements are correct?

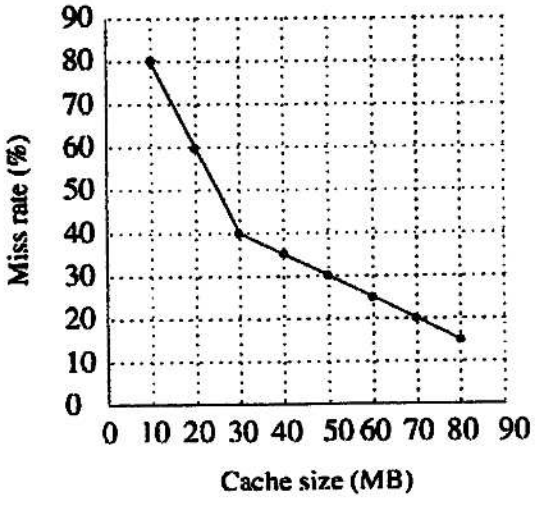
(a) For a single-cycle CPU where the instruction with the longest latency determines the clock cycle time, the clock cycle time is 350ps.
(b) For a classic MIPS CPU with a 5-stage pipeline, the clock cycle time can be 200ps.
(c) It takes 3000ps to execute the code sequence below using the single-cycle CPU.
(d) It takes 1000ps to execute the code sequence below using the pipelined MIPS CPU

```
1. lw   $t1, 0($s1)
2. sw   $s1, 0($s2)
3. add  $t2, $s2, $s3
4. add  $t3, $s1, $s2
5. lw   $t1, 0($t2)
```

6. Which of the following statements are *correct*?
(a) The number of pipeline stages affects latency, not throughput; thus pipelining improves the performance of a processor by decreasing the latency of a job (i.e., an instruction) to be done.
(b) For a given program, its average cycles per instruction (CPI) is affected not only by the instruction set architecture, but also by the compiler used.
(c) By changing the clock frequency of a processor from 1.5 GHz to 2 GHz, and also changing its supply voltage from 1 Volt to 1.25 Volt, the overall power consumption of this processor will theoretically increase by more than 2X.
(d) According to Amdahl's law, it is theoretically possible to achieve a 6X speedup on executing a program which is 87% parallelizable, by using a 16-core multiprocessor.

7. Consider a 1 KB, 4-way set associative cache (initially empty) with block size of 64 bytes. The main memory consists of 256 blocks and the request for memory blocks is in the following order: 0, 255, 1, 4, 3, 8, 142, 133, 159, 216, 113, 129, 63, 8, 17, 48, 32, 73, 92, 155. Which one(s) of the following memory blocks will NOT be in the cache if LRU replacement policy is used?
(a) 3
(b) 8
(c) 133
(d) 216

8. A file system uses an in-memory cache to cache disk blocks. The miss rate of the cache is shown in the figure below. The latency to read a block from the cache is X ms and to read a block from the disk is Y ms; besides, the cache size is Z MB (in multiples of 10 MB). Assume that the cost of checking whether a block exists in the cache is negligible.



Which one(s) of the following configurations can ensure an average read latency of 8 ms or less?
(a) X = 0.9, Y = 9, Z = 10
(b) X = 1.3, Y = 13, Z = 20
(c) X = 1.6, Y = 16, Z = 30
(d) X = 1.9, Y = 19, Z = 40

9. Which of the following statements (about virtual memory and page table) are *correct*?
(a) For virtual memory, write-back is more practical than write-through.
(b) Given a 32-bit virtual address space with 4 KB per page and 4 bytes per page table entry, the total page table size is 4 MB.
(c) It is possible to miss in cache and page table, but hit in translation look-aside buffer (TLB).
(d) It is possible to miss in TLB, but hit in cache and page table.

10. Which of the following statements are *correct*?
(a) RAID (redundant array of inexpensive/independent disks) can enhance the reliability/availability of data storage, and can also boost the performance of data access.
(b) RAID 1 provides fault tolerance by replicating data to mirror disks.
(c) The advantage of RAID 4 over RAID 3 is on the block-level striping/interleaving of data across disks, so as to allow more parallel data accesses.
(d) The advantage of RAID 6 over RAID 5 is on the distribution of parity blocks across disks, so as to avoid a single parity disk from being the bottleneck.

11. An I/O device signals the CPU through a hardware interrupt when it completes an I/O operation. Which one(s) of the following process state transitions can be caused by the hardware interrupt?
(a) ready to running
(b) running to ready
(c) waiting to ready
(d) waiting to running

12. Regarding process scheduling in interactive computer systems, which one(s) of the following statements are generally correct?
(a) Interactive processes usually produce short CPU bursts.
(b) CPU-bound processes should be assigned to high priorities so that they can complete as soon as possible.
(c) I/O-bound processes suffer from starvation with first-come first-serve scheduling.
(d) Shortest-job-first is a strategy to improve waiting time of processes.

13. Which one(s) of the following operations involve at least one system call?
(a) Reading a record from a file.
(b) Copying a string.
(c) Creating a new process.
(d) Displaying a window on the screen.

14. Which one(s) of the following statements adequately describe the test-and-set instruction for process synchronization?
(a) It does not work in multi-processor environments.
(b) It can all be implemented in the user space, provided that the lock variable is in a shared memory region.
(c) It does not waste any CPU cycles when a process cannot acquire a lock.
(d) The CPU must guarantee that the test-and-set instruction is an atomic operation.

15. Which one(s) of the following can cause thrashing in a virtual memory system?

(a) Decreasing the degree of multiprogramming
(b) Increasing the size of the page file (or swap partition)
(c) Under-clocking the CPU
(d) Removing one half of the memory chips form the system

16. Suppose that the application of a computer spends 10% of its time on I/O and 90% of its time on CPU. If we improve the performance of the computer's CPU by 100 times, what would be the overall performance improvement?
(a) Less than 100%
(b) Between 5 times and 10 times
(c) Between 15 times and 50 times
(d) More than 50 times

17. In designing a storage subsystem, which of the following are likely consequences of increasing the memory (RAM) size of a computer?
(a) Disk traffic becomes dominated by writes
(b) Random disk seeks can be largely eliminated
(c) Use of journaling file system in dealing with system crashes becomes unnecessary
(d) The performance overhead in using disk encryption can be largely eliminated

18. In practice, which of the following operations can be efficiently carried out without perceivable overhead due to accessing file data blocks?
(a) Moving files from a hard disk to an USB thumb drive
(b) Moving files between directories on the same disk partition
(c) Moving files between directories on different disk partitions
(d) Deleting files on a hard disk

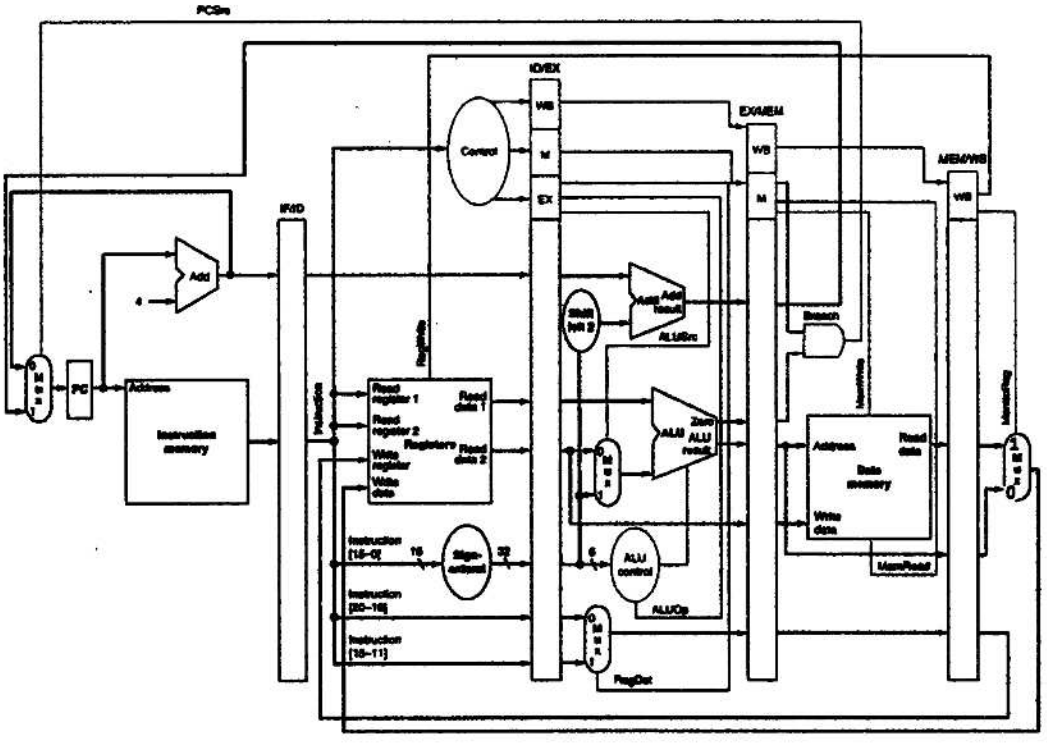
19. Which of the following security measures are an example of the principle of least privileges?
(a) Installing antivirus software on a system
(b) Set up firewall rules to block unwanted network connections
(c) Carry out penetration test on a system
(d) Periodically running system updates

20. Which of the following security measures can help thwart the threat of buffer overflow attack?
(a) Use static code analysis to look for memory writes that go beyond array boundaries
(b) Randomize the base addresses of program libraries in the memory
(c) Randomize the base addresses of program stacks in the memory
(d) Develop applications in Java or Python

二、題組(20%)，共四個題組，每一題組內所有小題全答對得 5 分，答錯任一小題或未作答得 0 分。題組A包含題號 21~23，題組B包含題號 24~25，題組C包含題號 26~28，題組D包含題號 29~31。

A. Consider the Pipelined CPU with five stages (IF, ID, EXE, MEM, WB) shown below and the code sequence on its left-side. Please answer the questions below.

```
add  $s1, $t1, $t2
sub  $s1, $s1, $s2
lw   $s2, 0($s1)
add  $t1, $s1, $s2
sub  $t3, $t2, $s2
sw   $s1, 0($t3)
or   $t4, $t2, $s2
add  $t1, $s2, $s1
```

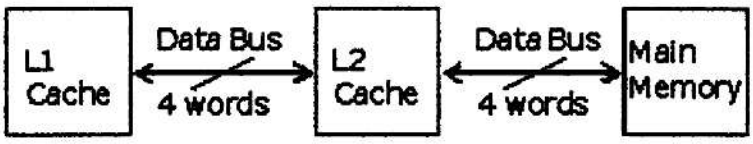


21. Assume forwarding and stall mechanisms have been designed (though it is not shown in the figure), which instruction is in IF stage when the code sequence runs to the 7th cycle?
    (a) or $t4, $t2, $s2
    (b) sw $s1, 0($t3)
    (c) sub $t3, $t2, $s2
    (d) add $t1, $s1, $s2

22. With the same assumption as question 21, which instruction is in EXE stage when the code sequence runs to the 7th cycle?
    (a) or $t4, $t2, $s2
    (b) sw $s1, 0($t3)
    (c) sub $t3, $t2, $s2
    (d) add $t1, $s1, $s2

23. Assume only stall mechanism has been designed (i.e., no forwarding paths) and assume register read and write can be done in the same cycle, which instruction is in MEM stage when the code sequence runs to the 7th cycle?
    (a) or $t4, $t2, $s2
    (b) sub $t3, $t2, $s2
    (c) lw $s2, 0($s1)
    (d) sub $s1, $s1, $s2

B. A computer system has an L1 cache, an L2 cache, and a main memory unit connected as shown below. The block size is 16 words for the L1 cache, and is 4 words for the L2 cache; the main memory is 4-word wide. The access times are 2 ns, 20 ns, and 200 ns for the L1 cache, L2 cache, and main memory, respectively.



24. When the processor requests some 4-word data, but there is a miss in the L1 cache and a hit in the L2 cache, how much is the total required time for data transfer upon this request?
(a) 20 ns
(b) 22 ns
(c) 80 ns
(d) 82 ns

25. When the processor requests some 4-word data, but there is a miss in both of the L1 cache and the L2 cache, and then a hit in the main memory, how much is the total memory access time for this request?
(a) 220 ns
(b) 222 ns
(c) 282 ns
(d) 880 ns

C. The following code fragments show a solution of the bounded-buffer problem. Producer processes and consumer processes share a buffer of N items. Items in the buffer are managed in a first-in first-out manner. A consumer removes items form the buffer, one at a time, and it waits if there is nothing in the buffer. Analogously, a producer appends items to the buffer, one at a time, and it waits if the buffer has no free space. Let `empty`, `full`, and `mutex` in the code fragments be semaphores. The buffer can store up to 10 items. Answer the following questions:

Producer process	Consumer process

`do {`
`  // produce an item`
`  wait (empty);`
`  wait (mutex);`
`  // append the item to the buffer`
`  signal (mutex);`
`  signal (full);`
`} while (true);`
	`do {`
	`  wait (full);`
	`  wait (mutex);`
	`  // remove an item from buffer`
	`  signal (mutex);`
	`  signal (empty);`
	`  // consume the removed item`
	`} while (true);`

26. What is the initial value of the semaphore `empty`?
(a) 0
(b) 1
(c) -1
(d) None of the above

27. What is the initial value of the semaphore `full`?
(a) 0
(b) 1
(c) -1
(d) None of the above

28. What is the initial value of the semaphore `mutex`?
    (a) 0
    (b) 1
    (c) -1
    (d) None of the above

D. Following is a C program that encrypts a file with AES-256 in cipher block chaining (CBC) mode. The AES encryption is based on the OpenSSL library.

```
01    #include <stdio.h>
02    #include <string.h>
03    #include <string>
04    #include <openssl/evp.h>
05    #include <openssl/aes.h>
06    #include <openssl/err.h>
07    #include <openssl/conf.h>
08    #include <openssl/rand.h>
09    #include <sys/types.h>
10    #include <sys/stat.h>
11    #include <fcntl.h>
12    #include <unistd.h>
13    #include <inttypes.h>
14    #include <assert.h>
15
16    using namespace std;
17
18    #define BUF_SIZE 16*1024
19
20    /* A 256 bit key */
21    static const unsigned char key[] = {
22      0x00, 0x11, 0x22, 0x33, 0x44, 0x55, 0x66, 0x77,
23      0x88, 0x99, 0xaa, 0xbb, 0xcc, 0xdd, 0xee, 0xff,
24      0x00, 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07,
25      0x08, 0x09, 0x0a, 0x0b, 0x0c, 0x0d, 0x0e, 0x0f
26    };
27
28    unsigned char iv[16];
29
30    EVP_CIPHER_CTX *ctx;
31
32    void encrypt_file(const char* src_file, const char* dst_file)
33    {
34      int err_code;
35      int fdSrc, fdDst;
36      unsigned char plaintext[BUF_SIZE];
37      unsigned char ciphertext[BUF_SIZE];
38      int bytes_read, ciphertext_len;
39
40      fdSrc = open(src_file, O_RDONLY);
41      fdDst = open(dst_file, O_CREAT | O_WRONLY, 0600);
42      RAND_bytes(iv, 16);
43      write(fdDst, iv,  sizeof(iv));
44      EVP_EncryptInit_ex(ctx, EVP_aes_256_cbc(), NULL, key, iv);
45
46      while( (bytes_read = read(fdSrc, plaintext, BUF_SIZE))>0 ) {
47          int ciphertext_len;
```

```
48            EVP_EncryptUpdate(ctx, ciphertext, &ciphertext_len, plaintext, bytes_read);
49            write(fdDst, ciphertext, ciphertext_len);
50        }
51
52        EVP_EncryptFinal_ex(ctx, ciphertext, &ciphertext_len);
53        write(fdDst, ciphertext, ciphertext_len);
54        close(fdSrc);
55        close(fdDst);
56    }
57
58    int main(int argc, char* argv[])
59    {
60        ERR_load_crypto_strings();
61        OpenSSL_add_all_algorithms();
62        OPENSSL_config(NULL);
63
64        ctx = EVP_CIPHER_CTX_new();
65        encrypt_file(argv[1], (string(argv[1]) + ".encrypted").c_str() );
66        EVP_CIPHER_CTX_free(ctx);
67        return 0;
68    }
```

29. Assume that we compile the C program into the executable file named `a.out`. On UNIX, if we type "`./a.out ./a.out`" on the command line and hit the enter key, what will be the name of the file created by the program?
    (a) ".encrypted"
    (b) "a.out"
    (c) ".a.out.encrypted"
    (d) "a.out.encrypted"

30. Assume that we use the program to encrypt a file of 163,900 bytes in size. How many times will `Line 49` be executed?
    (a) 1
    (b) 10
    (c) 11
    (d) 17

31. Assume that we use the program to encrypt a file of 500 MB in size. Which line of the code will generate significant amount of I/O traffic to the disk?
    (a) Line 40
    (b) Line 43
    (c) Line 46
    (d) Line 48