國立臺灣師範大學 113 學年度碩士班招生考試試題

科目：計算機系統　　適用系所：資訊工程學系

注意：1.本試題共 2 頁，請依序在答案卷上作答，並標明題號，不必抄題。2.答案必須寫在指定作答區內，否則依規定扣分。

1. (15 points) Please answer the following question about the **process** concept in the O.S. system.
   (a) (11 points) Draw a **Process State Diagram** and explain how a new job/process is transferred from state to state (starting from the first time a job is submitted to its termination).
   (b) (4 points) Use the Process State Diagram to explain the responsibility and differences between the **short-term scheduler** and the **long-term scheduler** in the process of scheduling.

2. (15 points) Please answer the following question about **synchronization**.
   (a) (4 points) What is a **critical section**?
   (b) (2 points) What is **busy waiting**?
   (c) (4 points) What are the advantages and disadvantages of busy waiting?
   (d) (5 points) How can we avoid busy waiting?

3. (10 points) Given that, a computer system with **single-level paging** uses a **Translation look-aside buffer** (TLB) to reduce the number of memory references. Assume that it takes 30 *ns* to search TLB and 90 *ns* to access the main memory. What is the **effective memory access time** if the TLB hit ratio is 70%? Show all your work.

4. (10 points) Given a computer system with a 32-bit virtual address, 4KB pages, and 8B per page entry of a page table. Suppose the number of bits of physical addresses is 48, and the system is byte-addressable. If **multiple-level paging** is implemented, please answer the following questions.
   (a) (3 points) What is the maximum number of (physical) page **frames** in the system, where each page frame is the container to store the data of one (virtual) page?
   (b) (3 points) What is the maximum number of **pages** for a process?
   (c) (4 points) Suppose that the multi-level paging is adopted. How many **levels** do we need?

5. (10 points) A system features a 256 Kbyte cache memory, and the cache is designed with "*K*"-way set associativity, utilizing the following address bits for cache access. What is the value of "*K*" in this system?

Tag	Set	Offset
31 - 14	13 - 4	3 - 0

6. (10 points) Examining the following code sequence in the MIPS five-stage pipeline, let's explore the implications of introducing pipeline stalls in the presence of data hazards (without utilizing forwarding). What would be the total cycle count required for the completion of the code sequence?

```
add $1, $2, $3
sub $4, $1, $5
add $6, $1, $7
add $8, $4, $1
sub $2, $7, $9
```

7. (10 points) Examine three processors, P1, P2, and P3, executing an identical instruction set. P1 operates at a clock rate of 3.6 GHz with a CPI of 1.8, P2 at 2.5 GHz with a CPI of 1.0, and P3 at a clock rate of 5.0 GHz with a CPI of 5.0. Identify the processor that demonstrates the highest performance in terms of instructions per second. Please illustrate your calculation to support your conclusion.

8. (10 points) In the following MIPS assembly loop, assume the initial value of register $t1 is set to *N*. Determine the total number of executed MIPS instructions for the loop.

```
LOOP: slt $t2, $0, $t1
      beq $t2, $0, DONE
      subi $t1, $t1, 1
      addi $s2, $s2, 2
      sll $t2, $s2, 1
      j LOOP
DONE:
```

9. (10 points) Assume the PC of the following branch instruction is 12. What is the new PC if the branch is taken?

```
beq $1, $2, 17
```