國立成功大學
111學年度碩士班招生考試試題

編　號：173

系　所：電機工程學系

科　目：計算機組織與作業系統

日　期：0219

節　次：第 1 節

備　註：不可使用計算機

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※ 考生請注意：本試題不可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. Assume the set of five processes have arrived at time 0, 1,2,3,4, respectively.

Process	Burst Time (ms)	Arrival Time
P1	10	0
P2	29	1
P3	3	2
P4	7	3
P5	12	4

Please calculate both of the average waiting time and average turnaround time for:

(a) FCFS

(b) SJF

(c) RR (Quantum = 10 ms)

(15%)

2. Consider the following segment table:

Segment	Base	Length
0	219	600
1	2300	14
2	90	100
3	1327	580
4	1952	96

What are the physical addresses for the following logical addresses?

(a) 0,430

(b) 1,10

(c) 2,500

(d) 3,400

(e) 4,112

(15%)

3. Please explain the meaning of Effective Access Time (EAT)? And please calculate the EAT of the following 1-level paging system. Ignore the overheads to revise the TLB and the page table, and suppose that each page fault involves page replacement (considering both swap-in and swap-out overhead).

TLB hit ratio = 90%
TLB access time = 200ns
Memory access time = 100μs
Page-fault ratio = 0.001%
To access a page on a disk = 15ms (including memory access time)
(You only need to list your calculation process, don't waste your time to calculate the final result.)
(10%)

4. Explain why interrupts are not appropriate for implementing synchronization primitives in multiprocessor systems.
(5%)

5. In order to ensure the proper execution of the operating system, we can use dual-mode with hardware support to differentiate among various modes of execution. Please describe the dual-mode operation and draw the transition from user to kernel mode.
(5%)

6. For the value 0x13579ACE, how would this value be stored in memory?
Assume the data stored at address 0 and word size is 4 bytes.
   (a) In a little-endian machine
   (b) In a big-endian machine
(10%)

7. Which of the following is/are true?
   (a) Two processor can be evaluated using MIPS(million instructions per second) to compare their overall performance
   (b) A right shift instruction can replace an integer division by a power of 2
   (c) Idea throughput of an single pipeline processor is 1*(number of pipeline stages) instruction per cycle
   (d) It is the principle of locality that gives us a chance to overcome the long latency of memory access.
   (e) Generally, increasing cache size can results in decreasing capacity misses
(10%, no partial point, no penalty)

8. Consider a five-stage RISC-V/MIPS pipeline processor, describe what will happen in each stage when executing the following instructions.
ld rd, immed(rs1) //load double word from mem[reg[rs1]+immed]
(10%)

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9. What does TLB stands for in the memory hierarchy system?
Describe how will TLB miss handler deal with a TLB miss.

(10%)

10. Dynamic branch prediction predicts branches at runtime using runtime information. Draw a 2-bit branch predictor scheme. Mark each state with predictions output and transition conditions.

(10%)