國立成功大學

111學年度碩士班招生考試試題

編　號：200

系　所：電機資訊學院-資訊聯招

科　目：計算機組織與系統

日　期：0219

節　次：第 1 節

備　註：不可使用計算機

編號： 200

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※ 考生請注意：本試題不可使用計算機。 請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. [20%] Determine whether each of the following statements is true (T) or false (F) ?
   a. [2%] When a computer has low utilization, they use little power.
   b. [2%] Consider the following performance measurement of a program, Computer A has higher MIPS, but Computer B is faster.

Measurement	Computer A	Computer B
Instruction count	10 billion	8 billion
Clock rate	4 GHz	4 GHz
CPI	1.0	1.2

   c. [2%] Suppose the program counter (PC) is at address 0x00000600. It is possible to use one single branch-on-equal (beq) MIPS instruction to get to address 0x00020000.
   d. [2%] In IEEE 754 single precision floating-point format, the smallest normalized positive number is $0000_0001_0000_0000_0000_0000_0000_0000_2$.
   e. [2%] The IEEE 754 binary representation of -0.75_{10} is $10111111000000000000000000000000_2$.
   f. [2%] Compared with Physically Indexed Physically Tagged (VIPT) cache, the main advantage of Virtually Indexed Physically Tagged (VIPT) cache is that it has lower a miss rate.
   g. [2%] A fully-associative cache does not have conflict misses.
   h. [2%] GPU relies on deeply pipelined architecture to hide long latency of DRAM access latency.
   i. [2%] Given the Roofline model in Figure 1, Kernel 1 is memory bandwidth-limited.
   j. [2%] It is possible that TLB misses and page fault does not occur.

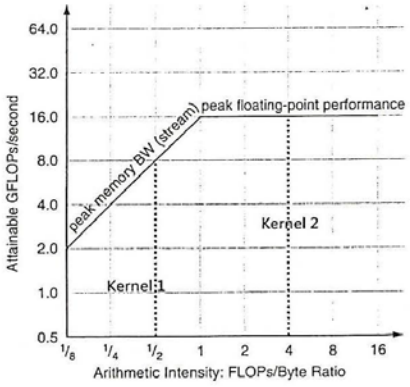


Figure 1.

2. [15%] Assume that the following MIPS code is executed on a pipelined processor with a 5-stage pipeline and a predict-taken branch predictor.

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```
            ADD R2, R1, R3
Label1 :    BEQ R2, R0, Label2     # not taken once, then taken
            LW   R3, 0(R2)
            BEQ R3, R0, Label1     # taken
            ADD R1, R3, R1
Label2 :    SW   R1, 0(R2)
```

The actual execution order of instruction is shown as follows:

```
            ADD R2, R1, R3
            BEQ R2, R0, Label2     # not taken
            LW   R3, 0(R2)
            BEQ R3, R0, Label1     # taken
            BEQ R2,R0, Label2      # taken
            SW   R1, 0(R2)
```

a. [5%] Assume **NO** forwarding and there are no delay slots. The branch result is determined at the **EX** stage. On your answer sheet, draw the following table and indicate the cycle at which each instruction is completed, assuming the first instruction is completed at cycle 5 (Hint: Draw the pipeline execution diagram for this code)

Execution Order	Completed at cycle?
ADD R2, R1, R3	5
BEQ R2, R0, Label	(1)
LW R3, 0(R2)	(2)
BEQ R3, R0, Label1	(3)
BEQ R2, R0, Label2	(4)
SW R1, 0(R2)	(5)

b. [10%] Assume **FULL** forwarding and there are no delay slots. The branch result is determined at the **ID** stage. On your answer sheet, draw the following table and indicate the cycle at which each instruction is completed, assuming the first instruction is completed at cycle 5 (Hint: Draw the pipeline execution diagram for this code.)

Execution Order	Completed at cycle?
ADD R2, R1, R3	5
BEQ R2, R0, Label	(1)
LW R3, 0(R2)	(2)
BEQ R3, R0, Label1	(3)
BEQ R2, R0, Label2	(4)
SW R1, 0(R2)	(5)

3. [15%] Cache are important to providing high-performance memory hierarchy to processors. Below is a list of 32-bit memory address reference, given as word address

   3, 180, 2, 43, 191, 88, 190, 14, 181, 88

   Answer the following questions.

   a. [5%] Using the above sequence of reference. Assume the cache is direct-mapped with 1-word block and has a total size of 8 words. Complete the following table by identifying whether each reference is hit or miss. What is the hit rate?

Addr.	3	180	2	43	191	88	190	14	181	88
H/M	Miss	Miss	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)

   b. [5%] Using the above sequence of reference. Assume the cache is two-way set associative with two-word block. and a total size of 8 words, used **LRU** replacement. Complete the following table by identifying whether each reference is hit or miss. What is the hit rate?

Addr.	3	180	2	43	191	88	190	14	181	88
H/M	Miss	Miss	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)

   c. [5%] Using the above sequence of reference. Assume a fully associate cache with two-word blocks and a total size of 8 words. Use **LRU** replacement. Complete the following table by identifying whether each reference is hit or miss. What is the hit rate?

Addr.	3	180	2	43	191	88	190	14	181	88
H/M	Miss	Miss	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)

4. [50%] For a computer system, its main job is input/output (I/O) and processing. In some cases, the main job is I/O, and the processing is merely identical. Please answer the following questions related to I/O subsystems of an operating system (OS).

   a. [5%] OS (especially device drivers) interacts with device controllers to perform I/O operations. What kinds of commands and data to a device controller can be issued in a device driver to accomplish an I/O transfer? Hint: The commands are often issued in the forms of processor instructions through special or standard I/O instructions.

   b. [5%] A special-purpose processor, called a direct-memory-access (DMA) controller, is often used to offload the burden of a central processing unit (CPU) for handling I/O operations. In such a computer system, the I/O operations can handle by CPU or DMA. Please specify which method (CPU-based or DMA-based) is suitable for latency-oriented I/O (for small-size data) and explain your answer.

   c. [5%] When a DMA controller is used to transfer data, it is often the case that the source and destination addresses of the transfer should be specified in physical memory addresses. Nevertheless, in a system with the virtual memory support, the mapping from virtual to physical addresses would be time-consuming jobs. What is the hardware device that can be used to help facilitate the mapping process?

   d. [6%] OS provides many services to enhance I/O performance. The descriptions of the three services are listed below. Please write down the name of the service (technique) based on its description.

i. [2%] A memory area that stores data while the data are being transferred from an application to a device.

ii. [2%] A region of fast memory that holds copies of data, and access to the copy is more efficient than access to the original data.

iii. [2%] A memory area that holds output for an I/O device that cannot accept interleaved data streams. Hint: Such an I/O device could serve one job at a time.

e. [4%] Asynchronous I/O can greatly improve I/O throughput in a computer. Which technique(s) (of the three services/techniques mentioned in the above question) can be adopted to implement an efficient asynchronous I/O operation? Explain your answer.

f. [5%] A swap space is often created by using disk space as an extension of main memory. In practice, a swap space can craved from the two approaches: a file system or a separate disk partition. Which approach can be used when the implementation efficiency is desired? Explain your answer.

g. [5%] What phenomenon will occur if a computer system is assigned with a fixed swap space and the degree of multiprogramming is increasing (by introducing new processes to the system)? Explain your answer.

h. [5%] Continue with the above question. The working-set model is proposed as a measure to prevent the above phenomenon from happening. We suppose a system with three processes, A, B, and C, and their working-set sizes (WSS) are WSS(a), WSS(b), and WSS(c), respectively. Also, we suppose the swap-space size of d. In what situation will OS suspend a process to improve the system performance? Please use a mathematical formula to define the situation with the relationship of WSS(a), WSS(b), WSS(c), and d.

i. [5%] Scheduling of disk I/O requests in a good order would greatly improve I/O efficiency. Given a multiprogramming environment with concurrent I/O, which disk scheduling family (among FCFS, SCAN, and LOOK families) will perform better? Explain your answer.

j. [5%] Continue with the above question. When the disk queue size is set to one, which disk scheduling family will perform better? Explain your answer.